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Jan 11, 2009 Lecture Series on VLSI Design by Dr.Nandita Dasgupta, Department of Electrical Engineering, IIT Madras. For more details on NPTEL visit

### **The effects of angle of incidence and temperature**

The Effects of Angle of Incidence and Temperature on Latchup in 65nm Technology J.M. Hutson 1, J.D. Pellish , G. Boselli2, R. Baumann2, R.A. Reed 1, R.D. Schrimpf , R

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CMOS technology : the problem and its cure. problem and its cure. by Ronald R. Troutman The Kluwer international series in engineering and computer science

### **Latch-up failure in cmos technology itu vlsi**

An analysis of Latch-Up failure, an effect of parasitic bipolar transistors, in CMOS Technology.

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This paper is a review of the latchup phenomena in past and present CMOS technologies. Both static and transient characterization techniques are described, as well as

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Jun 17, 2012 The CMOS structure is analyzed and the PNP and NPN latching transistors are identified. The CMOS latch schematic is drawn and the triggering methods are

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Latchup in CMOS technology. Kluwer Academic Publishers (1986) T. Aoki; A practical high-latchup immunity design methodology for internal circuits in the standard cell

### **Citeseerx 1.1 cmos latchup**

The pnp and npn transistors can be natural to the technology, or parasitic devices. In CMOS technology, testing and tools. 1.1.1 CMOS Latchup What is Latchup?

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A latch-up is a type of short circuit which can occur in an integrated circuit (IC). More specifically it is the inadvertent creation of a low- impedance path between

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### **Latchup -**

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Transient-Induced Latchup in CMOS Technology: Physical Mechanism and Device Simulation Ming-Dou Ker and Sheng-Fu Hsu Nanoelectronics and Gigascale Systems Laboratory

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### **Cmos - wikipedia, the free encyclopedia**

Complementary metal oxide semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers

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