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Failure analysis and solutions to overcome latchup

Latchup in CMOS technology. Kluwer Academic Publishers (1986) T. Aoki; A practical high-latchup immunity design methodology for internal circuits in the standard cell

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Why a book on Iatchup? Latchup has been, and continues to be, a potentially serious CMOS reliability concern. This concern is becoming more widespread

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Latchup -

All CMOS ICs have latch-up paths, but there are several design techniques that reduce susceptibility to latchup.

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An analysis of Latch-Up failure, an effect of parasitic bipolar transistors, in CMOS Technology.

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Latchup in cmos technology: the problem and its

A reviewer. This book is the first book on CMOS latchup by an earlier researcher in the field. My good friend Ron Troutman was highly respected internationally.

New transient characterization of latchup

This paper presents an analysis of the latchup development in CMOS integrated circuits. It sets out the time resolution of the triggering relevant to the differ

The latchup risk of cmos- technology in space |

The use of CMOS technology in space needs a careful evaluation of the latchup risk. The radiation tolerance is studied here for a standard 1.0 [μ]m high density

Citeseerx 1.1 cmos latchup

The pnp and npn transistors can be natural to the technology, or parasitic devices. In CMOS technology, testing and tools. 1.1.1 CMOS Latchup What is Latchup?

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Cmos latch-up - youtube

Jun 17, 2012 The CMOS structure is analyzed and the PNP and NPN latching transistors are identified. The CMOS latch schematic is drawn and the triggering methods are

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What is cmos latch up - answers.com

What is CMOS latch up? cmos technology is used in low power applications in vlsi and also CMOS is an acronym for complementary metal oxide semiconductor,

Transient-induced latchup in cmos technology:

Transient-Induced Latchup in CMOS Technology: Physical Mechanism and Device Simulation Ming-Dou Ker and Sheng-Fu Hsu Nanoelectronics and Gigascale Systems Laboratory

Learn and talk about latchup, integrated circuits

All CMOS ICs have latch-up paths, but there are several design techniques that reduce susceptibility to latchup. [5] [6] [7] In CMOS technology, there are a number of

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Interest in latchup is being renewed with the evolution of complimentary metal-oxide semiconductor (CMOS) technology, metal-oxide-semiconductor

The effects of angle of incidence and temperature

The Effects of Angle of Incidence and Temperature on Latchup in 65nm Technology J.M. Hutson 1, J.D. Pellish , G. Boselli2, R. Baumann2, R.A. Reed 1, R.D. Schrimpf , R

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The presence of active bipolar transistors in a BiCMOS technology increases the latchup susceptibility compared to pure CMOS processes, due to the injection of

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Latch-up - wikipedia, the free encyclopedia

A latch-up is a type of short circuit which can occur in an integrated circuit (IC). More specifically it is the inadvertent creation of a low- impedance path between

Cmos - wikipedia, the free encyclopedia

Complementary metal oxide semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers